Technical Information

Programmable Signal Gating Module

Summary

Hiden Analytical's new Programmable Signal Gating Module provides a significant enhancement to the 7U series of mass spectrometers (models EPIC / IDP / SIM / EQS / MAXIM / PSM and EQP) for time resolved applications. The 7U series currently operate with 1 microsecond gating resolution with the gating signals being provided by the user through an appropriate combination of function generators.

The new Programmable Signal Gating Module includes firmware/hardware which provides the necessary timing circuitry for time resolved applications (gate / delay / foreground / background / invert) with 0.1 µs resolution and under full control of MASsoft software.

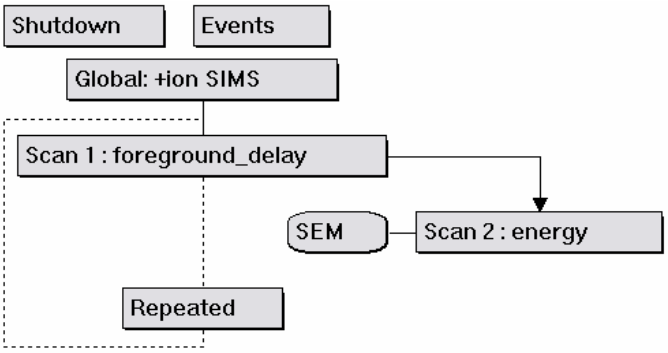
- It means no more function generators.
- It means the time event can be scanned with MASsoft.
- It is available with new systems and as a simple retrofit to your existing Hiden instrument.

Manufactured in England by:

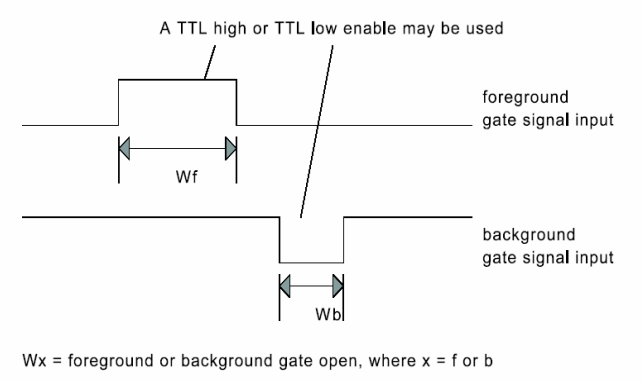
HIDEN ANALYTICAL LTD
420 Europa Boulevard, Warrington, WA5 7UN, England
t: +44 (0) 1925 445225 f: +44 (0) 1925 416518
e: info@hiden.co.uk w: www.HidenAnalytical.com

Features:

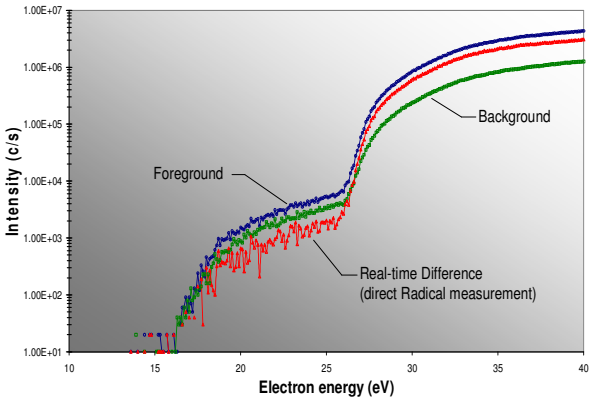
- Software gate control for data acquisition within a user defined time slice of a pulse cycle. 0.1µs resolution.



- Integral variable gate control delay for automatic data acquisition of a user defined time slice through the pulse cycle.



- Foreground and background data channels for simultaneous data acquisition of appearance potential beam-to-background signals in modulated molecular beam studies.



Programmable Signal Gating

Includes a sophisticated gating system including virtual foreground and background detectors to allow it to be used for time resolved measurements and to monitor differences between two time zones relative to a repeated event, automated data acquisition during beam on and beam off cycles in modulated molecular beam studies for example. Both the foreground delay and background delay timing may be scanned, enabling an automatic scan of the monitored time period across an event period using the mass spectrometer.

Molecular Beam Chopper

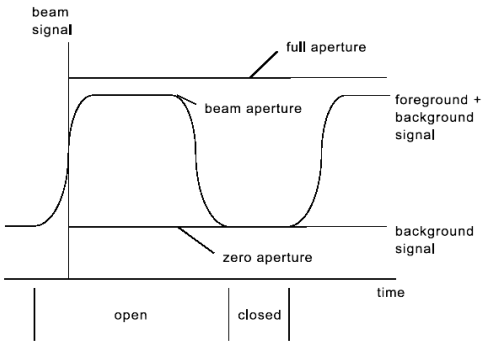


Figure 2 - Chopper vane cycle

Signal Gating

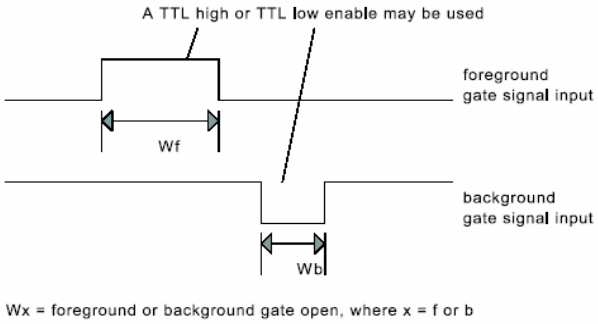


Figure 3 - Direct gating operation

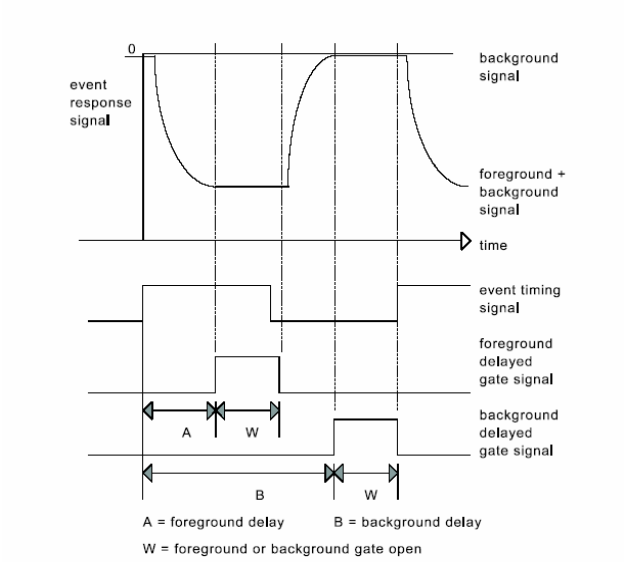


Figure 4 - Optimising gating delays

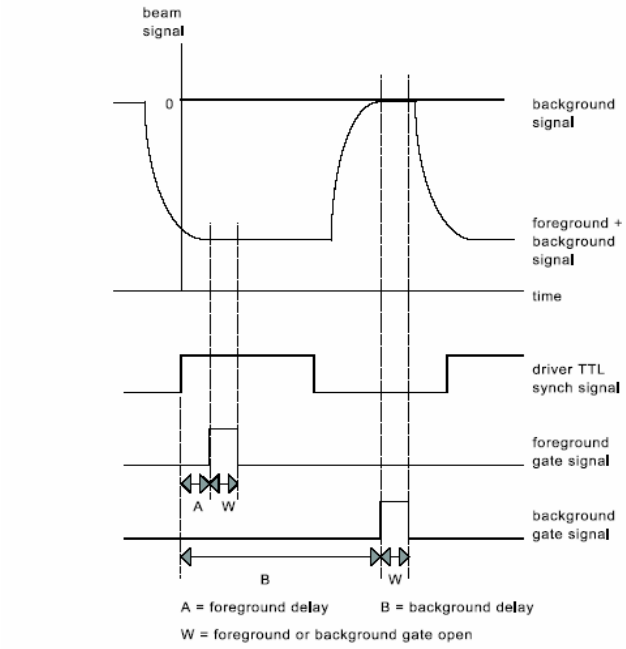


Figure 5 -Gate signal timing

Figures 2- 5 show examples of signal gate control, illustrating application of the comprehensive gating control variables that are included with Hiden's Programmable Signal Gating Module.

Automated signal gating - an example using Hiden's EQP mass/energy analyser.

Using the software control of Programmable Signal Gating Module the complete Ion Energy Distribution (IED) sequence shown in figure 7 was acquired automatically.

The Hiden Programmable Signal Gating variable 'foreground delay' was scanned from 0 to 2400µs in 100µs increments and an IED acquired from 2eV to 11eV in 0.5eV increments. A triangular waveform 500 Hz from 2V minimum to 8V maximum was used in this example to modulate the ion energy of a caesium source. EQP settings included extractor at -50V; detector dwell time 10ms; foreground gate scanned 0µs to 2400µs in 100µs increments; gate width 10µs. Full details of this study are available on request.

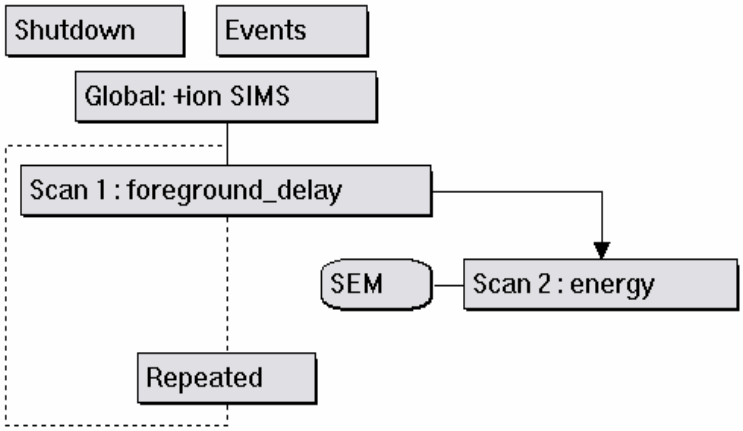


Figure 6 -Software control of detector gating

When viewed from the Ion Energy axis the profile of the average IED can be seen. Also evident is the triangular modulation of the energy. Each slice normal to the delay time axis shows the single energy profile of the ion source.

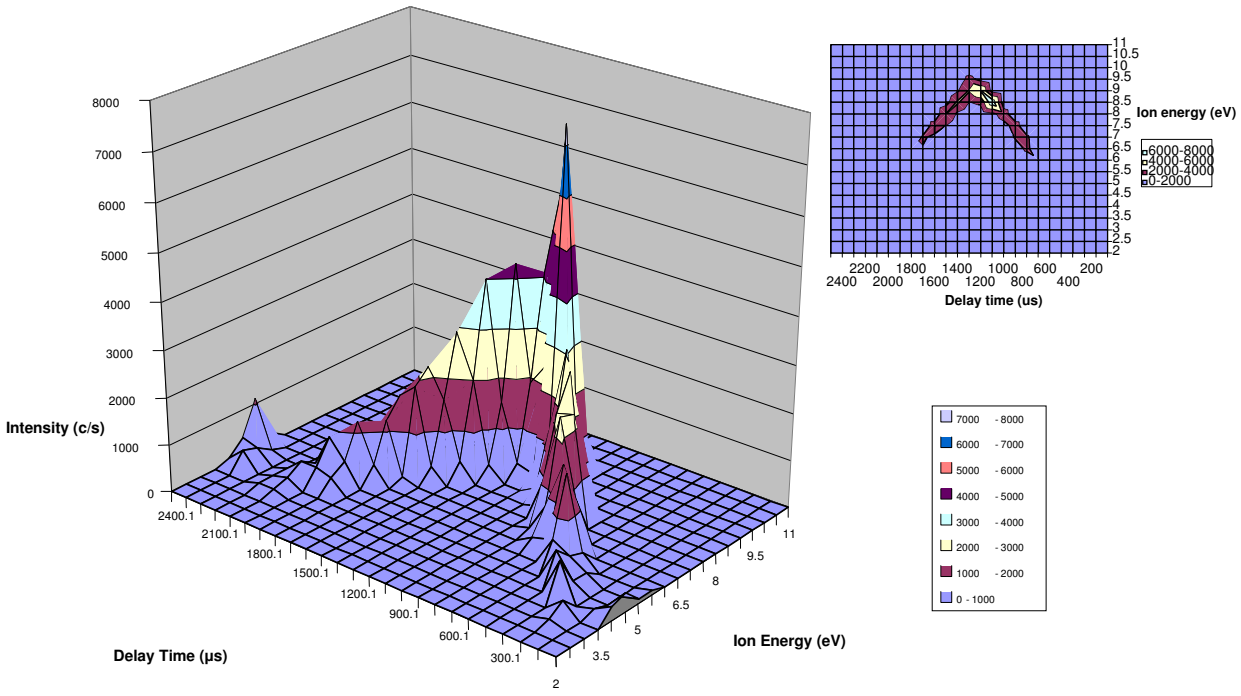


Figure 7 -IED sequence acquired using detector gating

Gating control variables available with Programmable Signal Gating

Gate Width:

Enables delayed gating and sets the width of both the foreground and background delayed gating pulses. When set to 0, delayed gating is disabled and gate signals directly control acquisition. When set to greater than 0, delayed gating is enabled and the value sets the width of the delayed gating pulse, and delayed gating pulses control acquisition.

Foreground Invert or Gating Invert

Controls the polarity of the foreground gating signal for direct gating and the active edge direction for delayed gating.

Foreground Delay or Gate Delay

Sets the delay between the trigger edge and the leading edge of the foreground delayed gating pulse.

Background Invert

Controls the polarity of the background gating signal for direct gating and the active edge direction for delayed gating.

Background Delay

Sets the delay between the trigger edge and the leading edge of the background delayed gating pulse.

Foreground and background gating may be enabled independently as positive or negative logic true, so that if the same gating signal is applied to both gate inputs, setting one of the invert variables to 0 and the other to 1 will enable foreground and background acquisition on alternate states of the signal.

Gating Specification

Gate signal inputs:

5V TTL logic levels - *low* = 0V to 1.0V. *high* = 2.4V to 5V minimum pulse width 50ns. maximum pulse width – unspecified.

Delay generator:

minimum delay = 0.1 µs. maximum delay = 6553.5 µs. resolution = 0.1 µs.

Width generator:

minimum width = 0 µs (a width of 0 µs will disable delayed gating) maximum width = 6553.5 µs, resolution = 0.1 µs.